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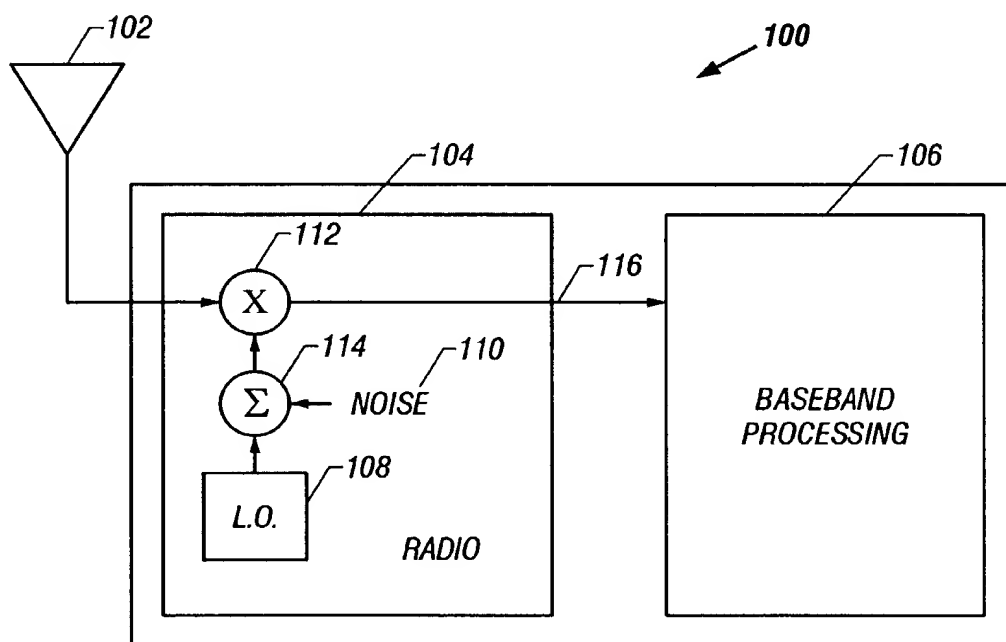


FIG. 1

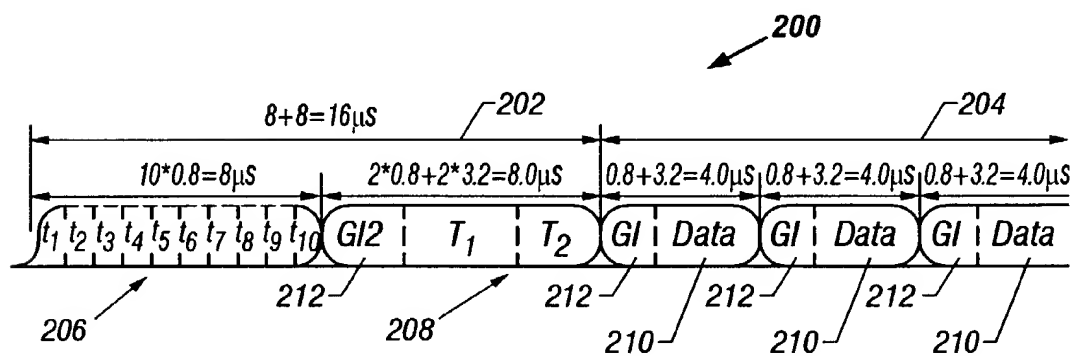


FIG. 2

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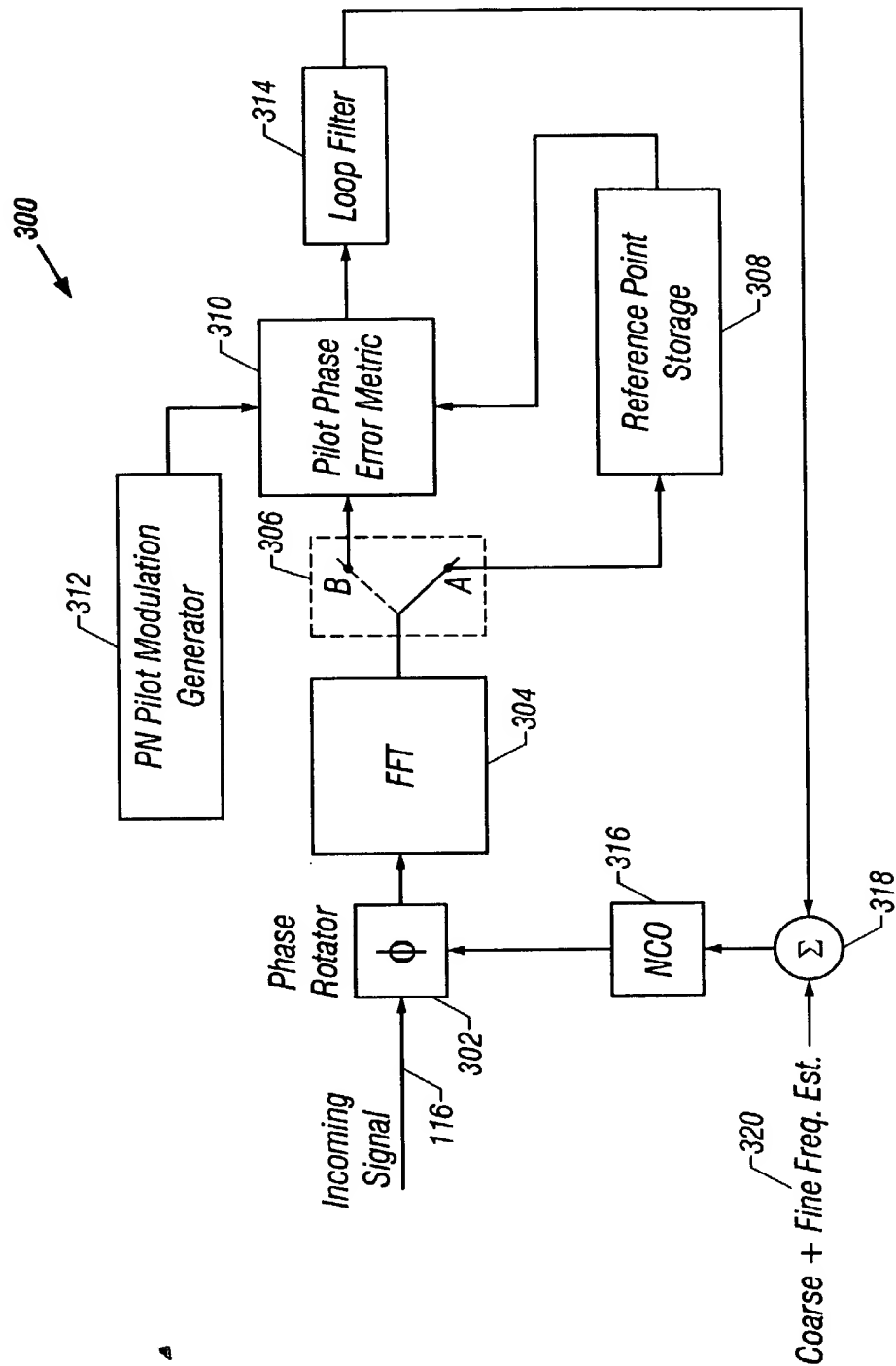


FIG. 3

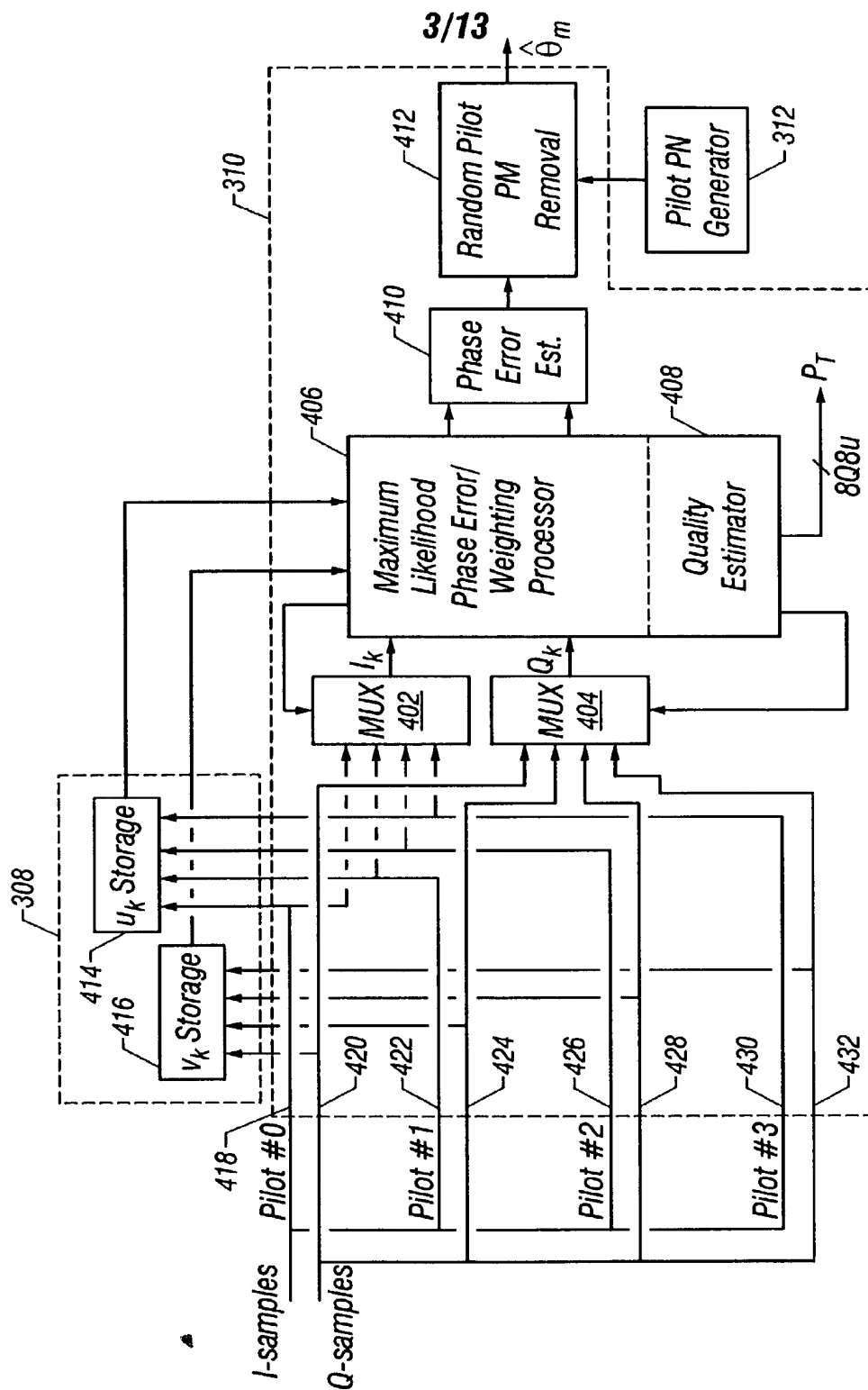
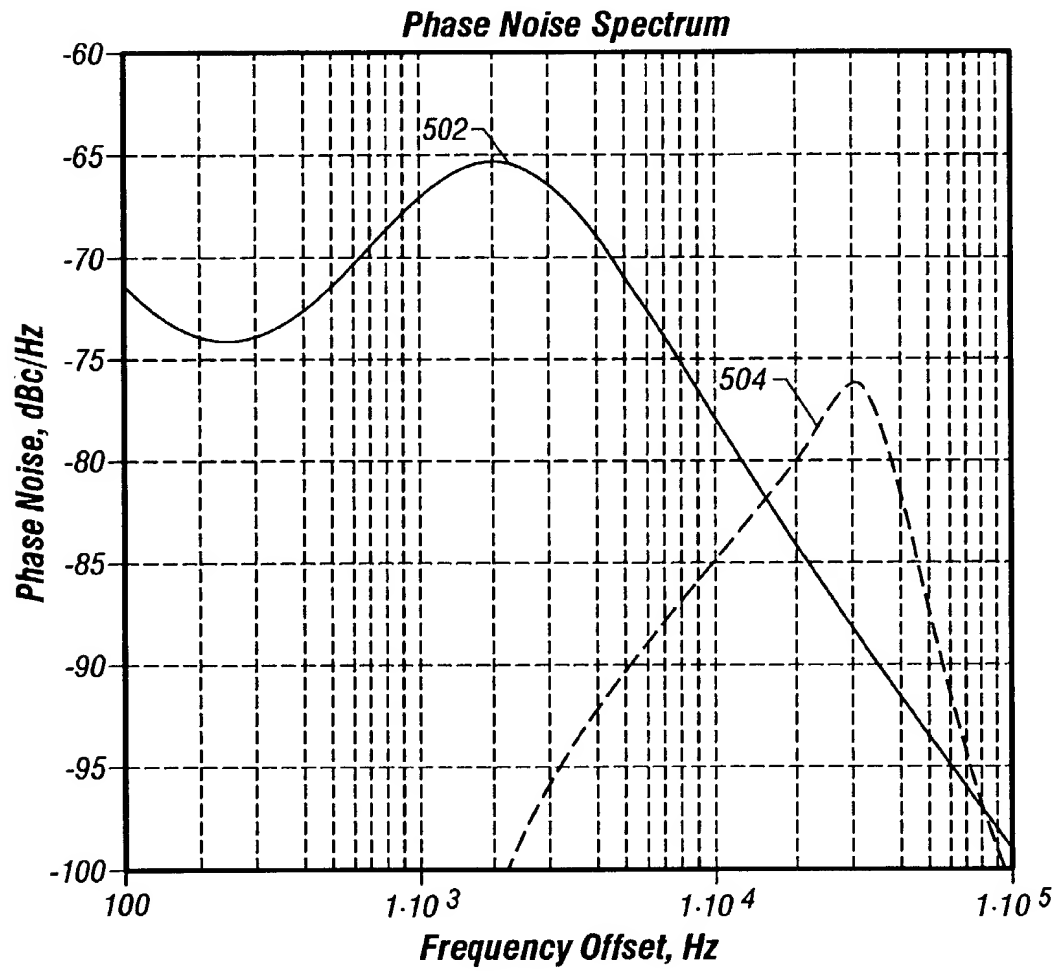


FIG. 4

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**FIG. 5**

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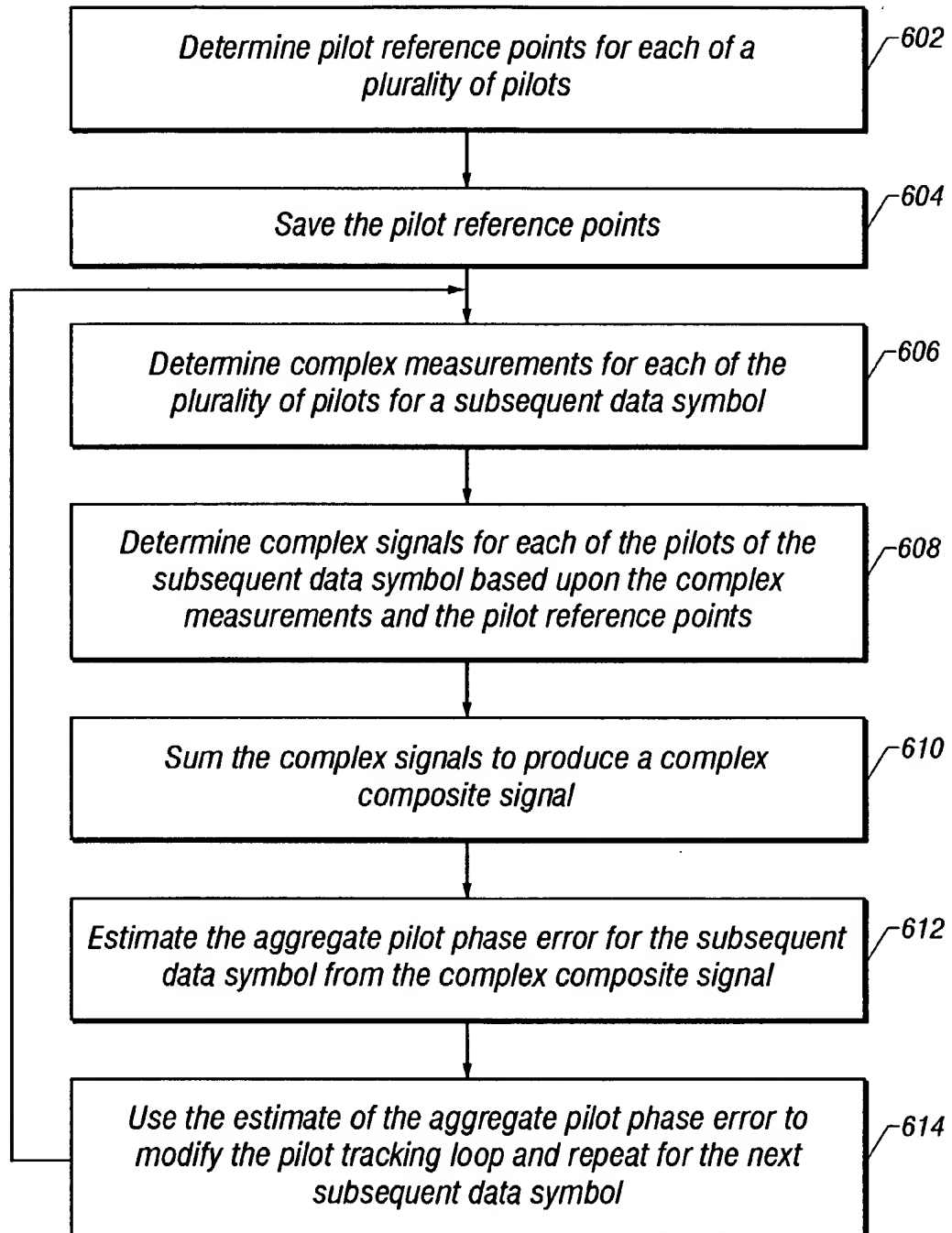


FIG. 6

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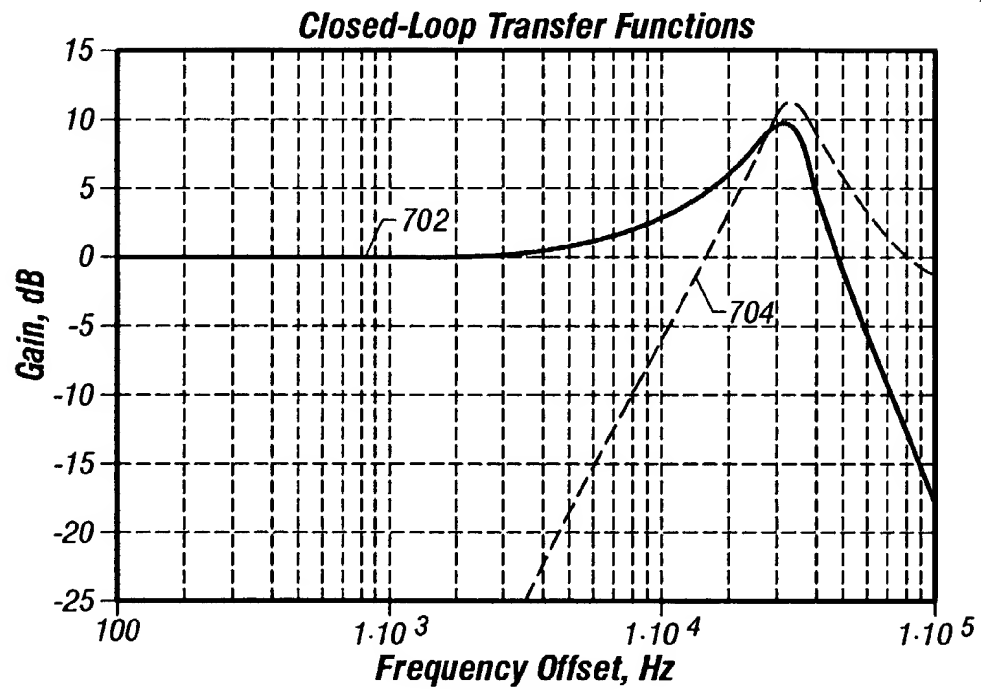


FIG. 7

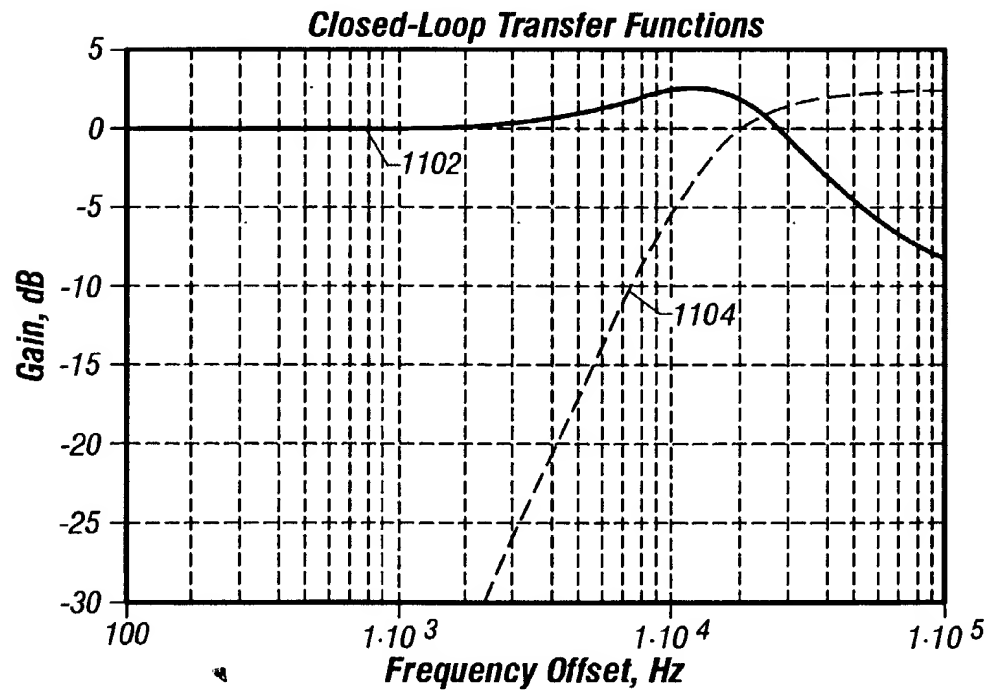


FIG. 11

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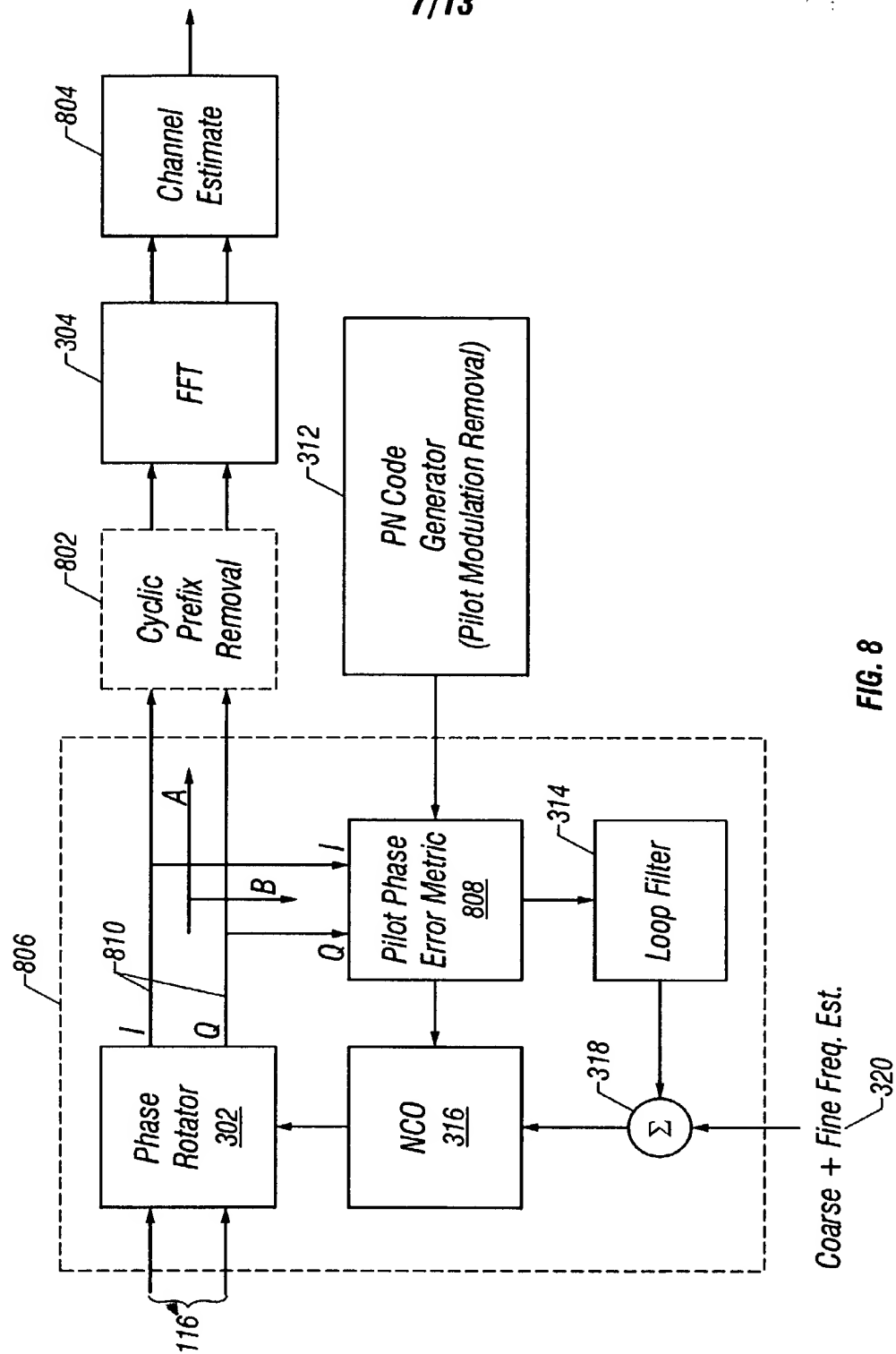


FIG. 8

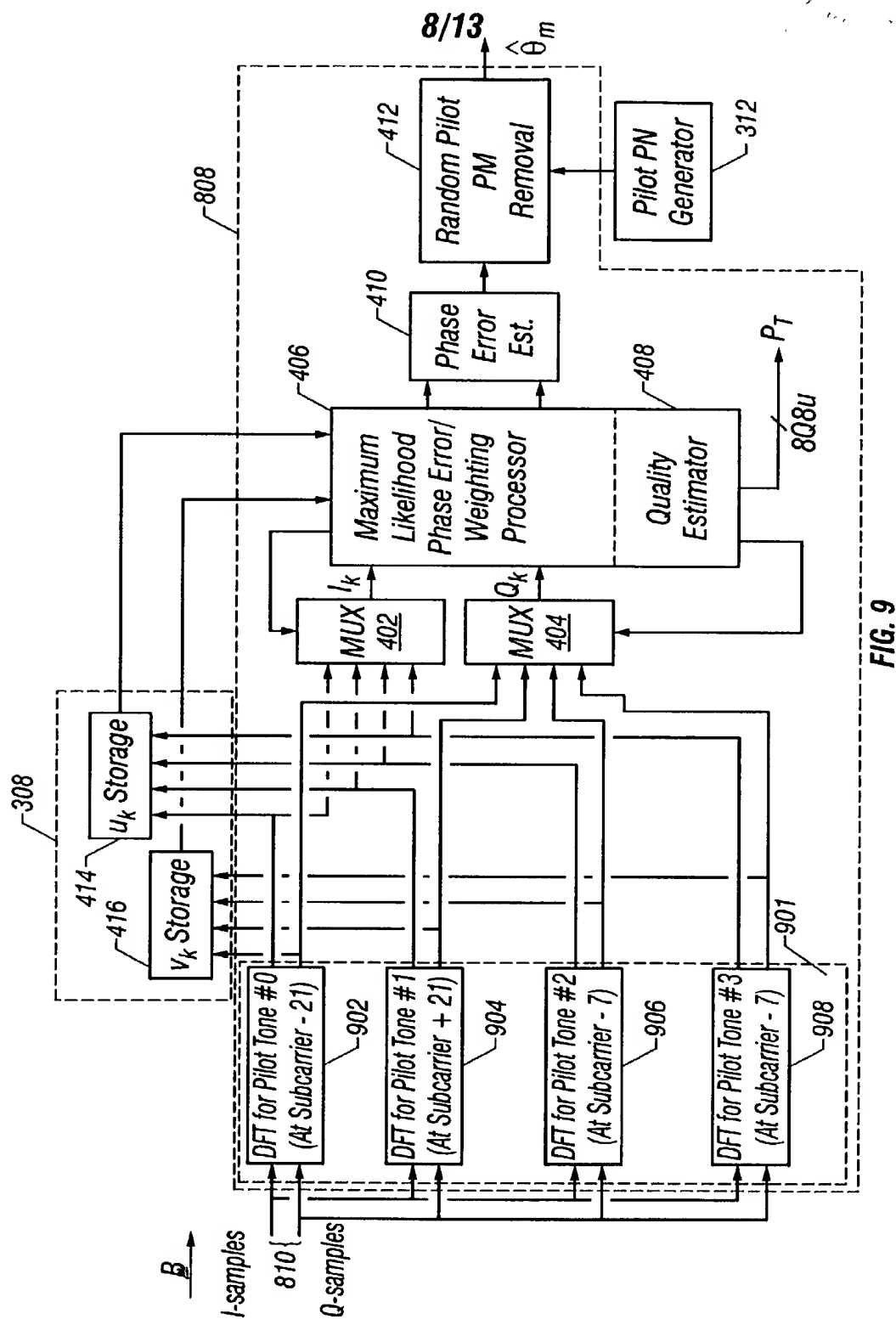


FIG. 9



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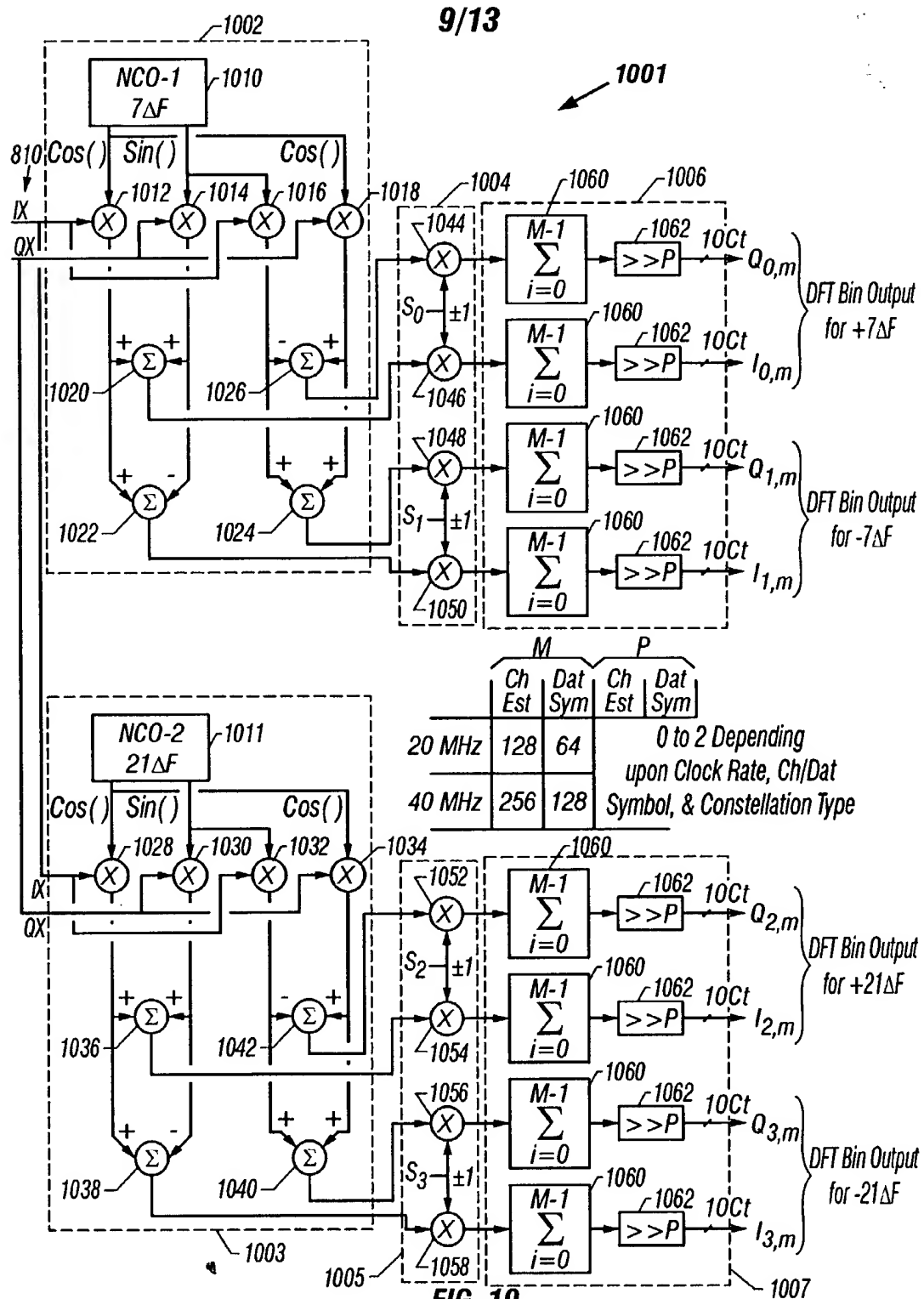


FIG. 10

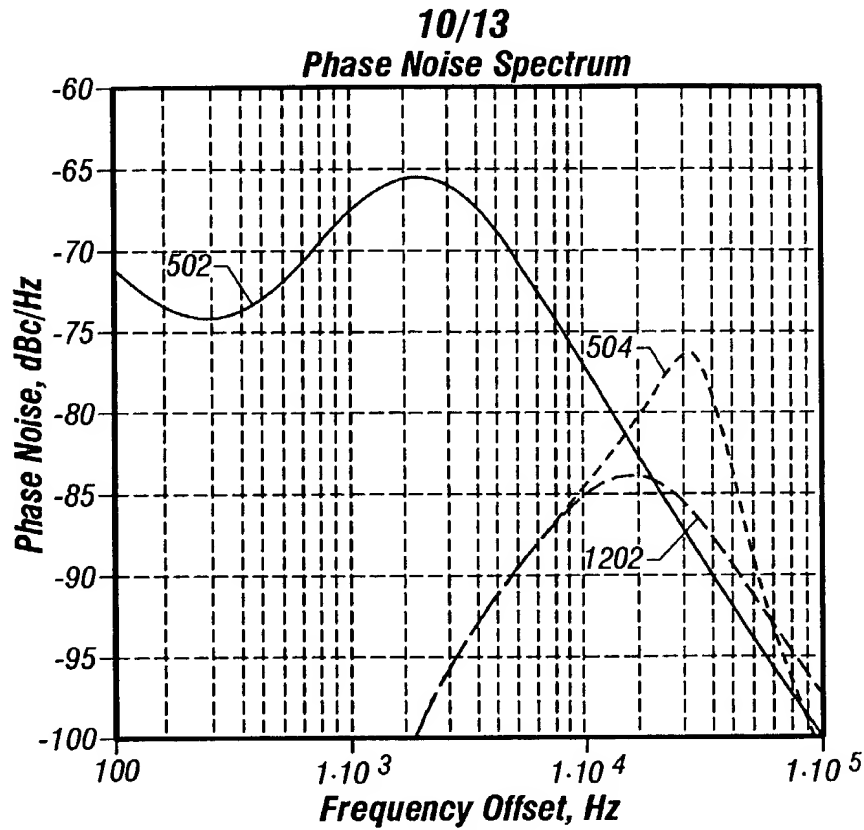


FIG. 12

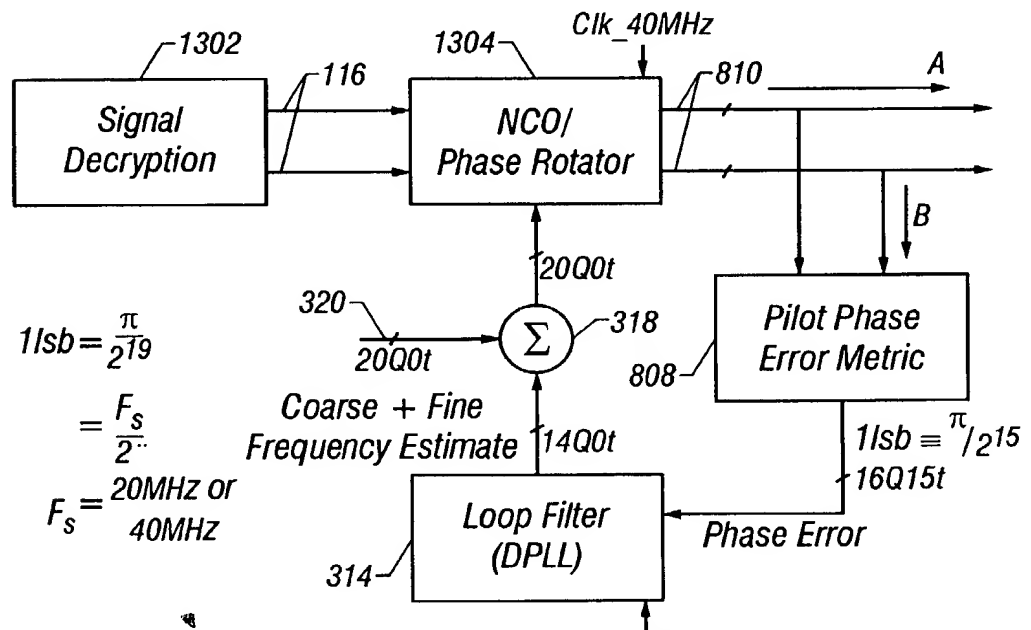


FIG. 13 Clk\_40MHz

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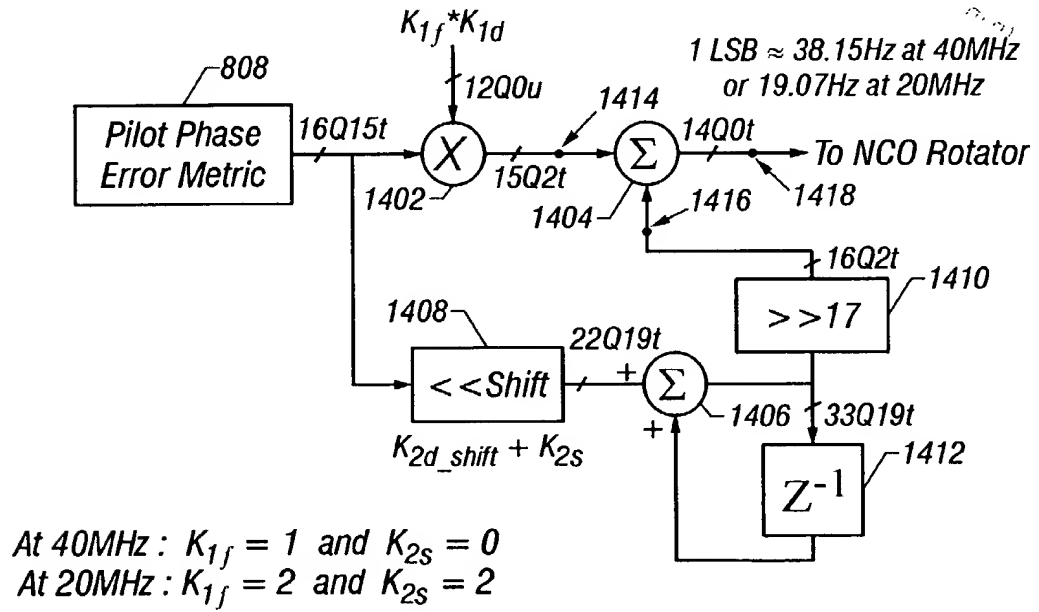


FIG. 14

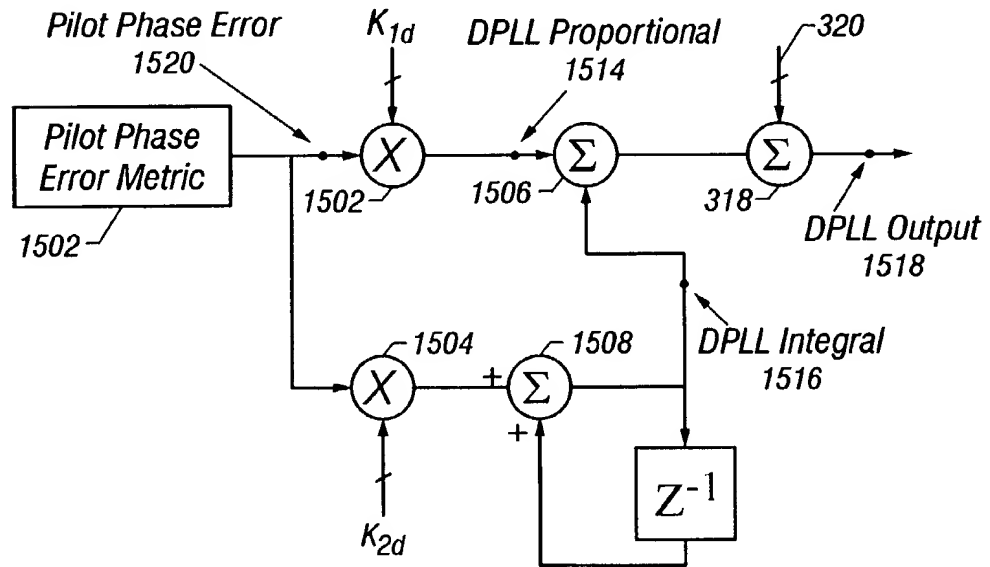


FIG. 15

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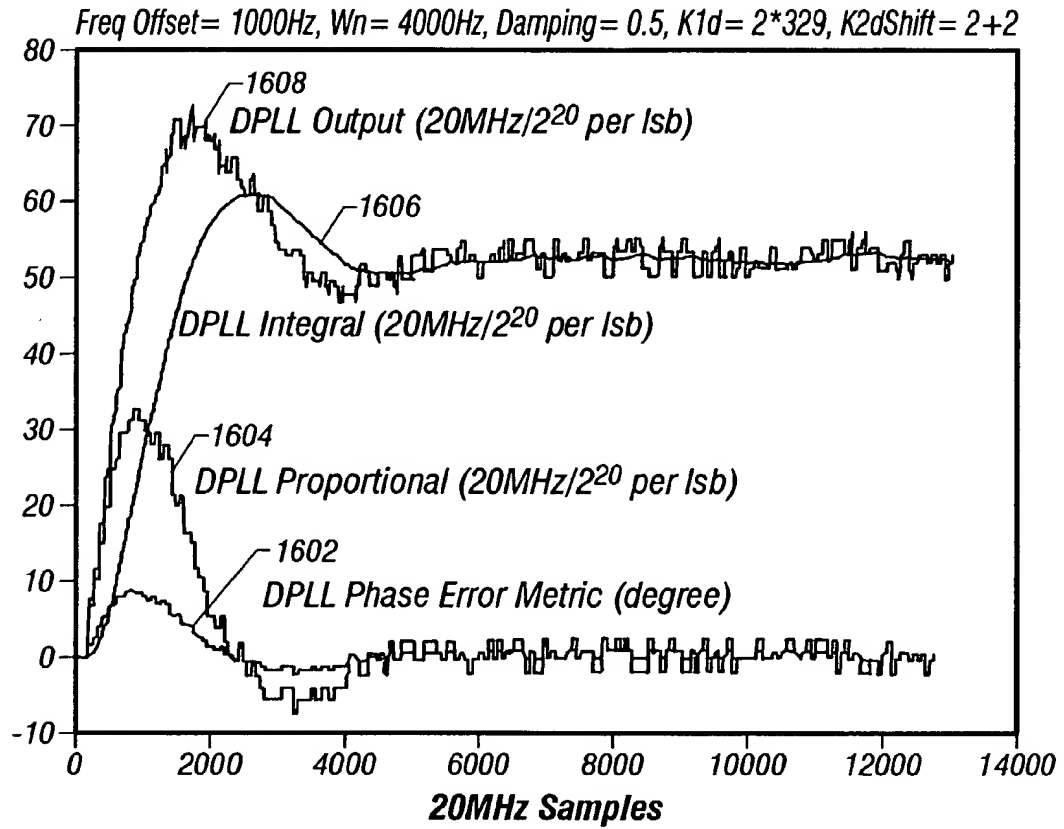


FIG. 16

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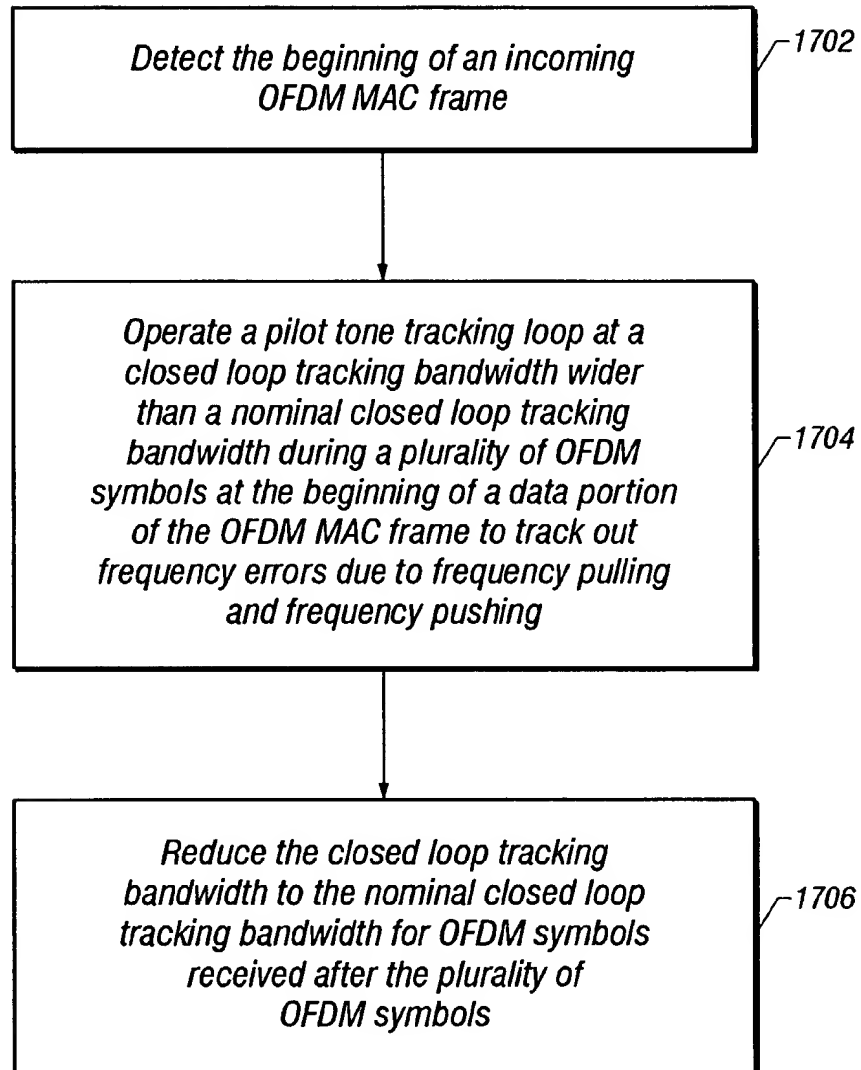


FIG. 17